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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,588	10/30/2003	Michio Oryoji	032072	7203

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EXAMINER	
NGUYEN, HA T	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 02/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,588	ORYOJI, MICHIO	
	Examiner	Art Unit	
	Ha T. Nguyen	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-20 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 October 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2-13+12-7-4.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1-20 are objected to because of the following informalities: In claim 1, lines 13 and 14, before "higher" and "a", respectively, insertion of –to a level—and –the top surface of--, in line 18, substitution of "higher than" with –above--, and in lines 19-20, "lower than" with –below—are suggested for clarity/correctness. Appropriate correction is required.

Claims 2-20 depend from claim 1, they are objected to for the same reason.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 5-6, 9-10, 13-14, and 17-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Watanabe et al. (USPN 6787907, hereinafter "Watanabe").

Referring to Figs. 1A-1F, 17AB-17BB, and related text, Watanabe discloses [Re claim 1] a method for manufacturing a semiconductor device including steps of forming a wiring by a dual damascene method, the method for manufacturing the semiconductor device comprising the steps of: forming a cap film 12, a first interlayer insulating film 13, an etching stopper film 14, a second interlayer insulating film15, and a hard mask in this order on a conductive layer 11; forming a via hole 55 which reaches the cap film in the hard mask, the second interlayer insulating film, the etching stopper film, and the first interlayer insulating film ; embedding an embedded material higher than the first interlayer insulating film and lower than a layered stack composed of the first interlayer insulating film, the etching stopper, and the second interlayer

insulating film in the via hole; forming a trench whose bottom is higher than an upper surface of the etching stopper film and lower than that of the embedded material in the second interlayer insulating film by etching the hard mask and the second interlayer insulating film, using a resist mask in which an opening for exposing the embedded material is formed (see Fig. 17AB); removing the resist mask and the embedded material ; etching the second interlayer insulating film again by using the hard mask as a mask; forming a wiring trench by removing the hard mask, and exposed parts of the etching stopper film, and the cap film; and embedding an electric conductive film 60 in the via hole and the wiring trench; [Re claim 2] a height of the embedded material is adjusted in said step of embedding the embedded material so that a bottom of the trench is lower than the upper surface of the embedded material even if the embedded material is etched when etching the hard mask and the second interlayer insulating film (see Fig. 17AB); [Re claims 5 and 6] wherein the etching stopper film and the hard mask are made of an identical material, silicon nitride; [Re claims 9-10 and 13-14] wherein the cap film, the etching stopper film and the hard mask are made of materials capable of being removed under an identical etching condition; silicon nitride; [Re claims 17-18] wherein said step of embedding the electric conductive film in the via hole and the wiring trench includes the steps of: forming a barrier metal film on the surface of the via hole and the wiring trench; and forming a wiring material on the barrier metal film; [Re claims 19-20] wherein said step of forming the wiring material includes the steps of: forming a seed film on the barrier metal film; and forming a metal film on the seed film by a plating method (see col. 8, line 27-col. 10, line 25).

Claim Rejections - 35 USC. § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103□ and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 3-4, 7-8, 11-12, and 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watanabe, as applied above, in view of (Applicants' admitted prior art , hereinafter "APA").

Watanabe discloses substantially the limitations of claims 3-4, 7-8, 11-12, and 15-16, as shown above.

But it fails to disclose expressly wherein the first and the second interlayer insulating films are SIOC group insulation films.

However, the missing limitation is well known in the art because APA discloses this feature (See the instant specification, page 2).

A person of ordinary skill is motivated to modify Watanabe with APA to obtain low dielectric constant dielectric without the corrosion effect caused by fluorine dopant.

Therefore, it would have been obvious to combine Watanabe with APA to obtain the invention as specified in claims 3-4, 7-8, 11-12, and 15-16.

6. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over APA in view of Li et al. (USPN 6794293, hereinafter "Li").

Referring to Figs. 6A-7D, and pages 2-3 of the instant specification, APA discloses [Re claim 1] a method for manufacturing a semiconductor device including steps of forming a wiring by a dual damascene method, the method for manufacturing the semiconductor device comprising the steps of: forming a cap film 102, a first interlayer insulating film 103, an etching stopper film 104, a second interlayer insulating film105, and a hard mask 107 in this order on a conductive layer 101; forming a via hole which reaches the cap film in the hard mask, the second

interlayer insulating film, the etching stopper film, and the first interlayer insulating film ; embedding an embedded material 109 in the via hole; forming a trench whose bottom is lower than that of the embedded material by etching the hard mask and the second interlayer insulating film, using a resist mask in which an opening for exposing the embedded material is formed; removing the resist mask and the embedded material; forming a wiring trench by removing the hard mask, and exposed parts of the etching stopper film, and the cap film; and embedding an electric conductive film 60 in the via hole and the wiring trench; [Re claim 2] a height of the embedded material is adjusted in said step of embedding the embedded material so that a bottom of the trench is lower than the upper surface of the embedded material even if the embedded material is etched when etching the hard mask and the second interlayer insulating film (see Fig. 7B); [Re claims 3-4] wherein the first and the second interlayer insulating films are SIOC group insulation films; [Re claims 5-8] wherein the etching stopper film and the hard mask are made of an identical material, silicon nitride; [Re claims 9-1 6] wherein the cap film, the etching stopper film and the hard mask are made of silicon nitride, materials capable of being removed under an identical etching condition (see col. 8, line 27-col. 10, line 25). But APA fails to disclose the claim height of the embedded material and etching the second interlayer insulating film again by using the hard mask as a mask. However, the missing limitations are well known in the art because Li et al. discloses these features (See Fig. 1C, 7E-7F). A person of ordinary skill is motivated to modify APA with Li to obtain controlled critical dimension.

[Re claims 17-20] The combined teaching of APA and Li does not disclose wherein said step of embedding the electric conductive film in the via hole and the wiring trench includes the steps of: forming a barrier metal film on the surface of the via hole and the wiring trench; and forming a wiring material on the barrier metal film; wherein said step of forming the wiring material includes the steps of: forming a seed film on the barrier metal film; and forming a metal film on the seed film by a plating method. However, the examiner takes Official Notice that when the embedded electric conductive film is Cu, as commonly used, a barrier layer and a seed layer on the barrier layer are normally used to electroplate Cu making devices of good quality at a lower processing cost.

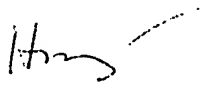
Therefore, it would have been obvious to combine APA with Li to obtain the invention as specified in claims 1-20.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ha T. Nguyen whose telephone number is (571) 272-1678. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM, except the first Friday of each bi-week. The telephone number for Wednesday is (703) 560-0528.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt, can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Ha Nguyen
Primary Examiner
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